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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,546	02/05/2004	Mauro Cerisola	4481-080	2813

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EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,546	CERISOLA, MAURO	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/5/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The application has not been checked to the extent necessary to determine the presence of all possible typographical and grammatical errors. However, Applicant's cooperation is requested in correcting any errors of which he/she may become aware in the application.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on February 5, 2004 was in compliance with the provisions of 37 CFR 1.97. Accordingly, the IDS is considered and an initiated copy of the IDS is accompanied with this Office Action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Joffe et al. (US 5,856,758) (hereinafter referred to as "Joffe").

Regarding claim 1, Joffe discloses a converter/circuit (see and compare Figs. 2, 5, and 6 of Joffe and the inventive figure, Fig. 4), wherein the converter includes: a differential amplifier (20) having non-inverting and inverting inputs (21, 22), and associated circuitry for applying an input voltage signal (Vin) to the converter and deriving from the associated circuitry an output signal current for driving a load (45); a sensing resistor (33) series connected with the load and having opposite first and second terminals for respectively applying voltages to first and second feedback loops (34/35); the loops being respectively associated with the non-inverting and inverting inputs of the differential amplifier; each of the loops including an intermediate tap (between resistors 31/34 and 32/35, respectively) connected to a respective input of the differential amplifier, and a first branch (upper or lower feedback path) including a first resistor (34 or 35) connected between the intermediate point associated with the particular feedback loop and the terminal of the sensing resistor (33) associated with the particular feedback loop; whereby the sensing resistor (33) is connected between the first branches of the first and second feedback loops; each of the loops also including a second branch having a second resistor (31/32) connected between the intermediate point associated with the particular feedback loop and an input port of the converter circuit; the first resistors (34/35) in the feedback loops have resistance values (R) that are of the same order of magnitude and are substantially higher than the resistance values of the sensing resistor and the load (column 3, line 42; column 4, lines 61-65;

and Fig. 2); whereby the current adapted to flow across the sensing resistor is an output current signal directly proportional to the input voltage signal applied between input ports of the second branches of the first and the second feedback loops.

Regarding claim 2, Joffe discloses the input voltage signal (Vin) is adapted to be applied to the input port of the second branch of said first feedback loop, and the input port of said second branch of said second feedback loop is connected to the ground (see Figs. 2, 5, & 6).

Regarding claim 3, Joffe discloses the input ports (21/22) of the second branches of said first and second voltage feedback loops are input ports for said conversion circuit having said input voltages signal applied therebetween in a differential arrangement.

Regarding claim 4, Joffe disclose the first resistors in said first branches of said first and second feedback loops have identical resistance values (R).

Regarding claim 5, Joffe discloses the first and second feedback loops include voltage dividers (31/34; and 32/35) having respective voltage divider ratios defined by said first resistor in said first branch and said second resistor in said second branch, and wherein said respective voltage dividers are the same for said first and second feedback loops.

Regarding claim 6, Joffe discloses the first branch in said first feedback loop is connected to the output of said differential amplifier (Figs. 2, 5, and 6).

Regarding claims 7 & 9, Joffe discloses the intermediate points (21/22) in the feedback loops are connected to the inputs of the differential amplifier (20).

Regarding claim 8, Joffe discloses the first branch of said second feedback loop is connected between said sensing resistor and said load (Figs. 2, 5, and 6).

Regarding claim 10, Joffe discloses the converter/circuit of claim 1 including a ramp signal generator (40) for applying to the input port of one of the second branches of one of said first and second feedback loops a ramp signal for gradually reducing said output current signal.

Regarding claim 11, Joffe discloses the converter includes a laser source (45) connected to the converter as the load and having an impedance Rt (Fig. 2).

Regarding claim 12, Joffe discloses (see Fig. 7 and the above Figs.) the converter/circuit of the above claims is a driver circuit for driving the load of claim 11, wherein the driver circuit being connected to between the output terminal of the differential amplifier and said sensing resistor and in series with the load 45 of claim 11.

Regarding claim 13, Joffe discloses a circuit comprising an output terminal (43) for connection to a load (45); an amplifier arrangement (20) having an output terminal and inverting and non-inverting input terminals (21/22), the amplifier arrangement being arranged for deriving at the output terminal thereof an output voltage having a magnitude directly proportional to the difference in the voltages at the inverting and non-inverting output terminals; first and second voltage dividers; a sensing resistor (33) connected between the circuit output terminal and the amplifier arrangement output terminal; a first feedback path (upper or lower path)connected between the output terminal of the amplifier arrangement and one of the input terminals of the amplifier arrangement; a second feedback path (lower or upper) connected between the output

terminal of the circuit and the other input terminal of the amplifier arrangement; the first feedback circuit being included in a first resistive voltage divider (31/34 or 32/35) connected between the circuit input terminal and the output terminal of the amplifier arrangement; the second feedback circuit being included in a second resistive voltage divider (32/35 or 31/34) connected between a further terminal and the circuit output terminal; the first voltage divider having a first tap (21 or 22) connected to drive the first input terminal of the amplifier arrangement; the second voltage divider having a second tap (22 or 21) connected to drive the second input terminal of the amplifier arrangement; the voltage dividers having voltage division factors and the sensing resistor having a value for causing the current flowing through the circuit output terminal into the load to be directly proportional to the difference in the voltages at the circuit input terminal and the further terminal; the resistance of the first voltage divider between the output and first input terminals of the amplifier arrangement and the resistance of the second voltage divider between the circuit output terminal and the second input terminal of the amplifier arrangement being on the same order of magnitude and much greater than the resistance of the sensor resistance (see column 3, line 42; column 4, lines 61-65; and Fig. 2).

Regarding claim 14, Joffe discloses the further terminal (the left side of the resister 31) of the circuit of claim 13 is at ground potential.

Regarding claim 15, Joffe discloses the further terminal (the left side of the resister 31) is connected to be responsive to a voltage source having a voltage other than ground (Vin).

Regarding claim 16, Joffe discloses the circuit of claim 13 including a bias source (135), the load (45) including a laser diode connected between the circuit output terminal and the bias source; the bias source, laser diode, circuit output terminal, sensing resistor and amplifier arrangement being arranged for causing current to flow from the bias source through the load, circuit output terminal and sensing resistor into the output terminal of the amplifier arrangement.

Regarding claim 17, Joffe discloses a circuit (Figs. 2, 5, and 6) comprising an output terminal (43) for connection to a load (45); an amplifier arrangement (20) having an output terminal and inverting and non-inverting input terminals (21-22), the amplifier arrangement being arranged for deriving at the output terminal thereof an output voltage having a magnitude directly proportional to the difference in the voltages at the inverting and non-inverting output terminals; first and second voltage dividers (31/34; and 32/35); a sensing resistor (33) connected between the circuit output terminal and the amplifier arrangement output terminal; a first feedback path (upper or lower) connected between the output terminal of the amplifier arrangement and one of the input terminals of the amplifier arrangement; a second feedback path (lower or upper) connected between the output terminal of the circuit and the other input terminal of the amplifier arrangement; the first feedback circuit being included in a first resistive voltage divider connected between the circuit input terminal and the output terminal of the amplifier arrangement; the second feedback circuit being included in a second resistive voltage divider connected between a further terminal and the circuit output terminal; the first voltage divider having a first tap (node 21 or 22) connected to drive the first input terminal of the

amplifier arrangement; the second voltage divider having a second tap (22 or 21) connected to drive the second input terminal of the amplifier arrangement; the voltage dividers having voltage division factors and the sensing resistor having a value (Ro) for causing the current flowing through the circuit output terminal into the load to be directly proportional to the difference in the voltages at the circuit input terminal and the further terminal; the first and second input terminals being respectively the non-inverting and inverting input terminals of the amplifier arrangement.

Regarding claim 18, Joffe disclose the further terminal (the left side of the resister 31) is connected to ground and the circuit input terminal is connected to a voltage source (Vin).

Regarding claim 19, Joffe discloses the further (the left side of the resister 31) and input terminals are respectively connected to first and second voltage sources (240 of Fig. 7).

Regarding claim 20, Joffe discloses the amplifier arrangement is arranged so the gain factor polarity between inverting and non-inverting input terminals and the output terminals of the amplifier arrangement causes the output current of the amplifier arrangement to be directly proportional to and have the same polarity as (V.sub.A-V.sub.B), where V.sub.A and V.sub.B are respectively the voltages at the non-inverting and inverting input terminals.

Regarding claim 21, Joffe discloses the load (45) includes a laser diode having first and second electrodes respectively connected to be responsive to the voltages of a non-grounded terminal of a DC voltage source and the circuit output terminal, the DC

voltage source polarity and the laser diode polarity being such that DC current is adapted to flow between the DC voltage source ungrounded terminal and the circuit output terminal via the laser diode.

Regarding claim 22, Joffe discloses the amplifier arrangement is arranged so the gain factor polarity between inverting and non-inverting input terminals and the output terminals of the amplifier arrangement causes the output current of the amplifier arrangement to be directly proportional to and have the same polarity as (V.sub.A-V.sub.B), where V.sub.A and V.sub.B are respectively the voltages at the non-inverting and inverting input terminals (see and compare the inventive Fig. 4 and the prior art figures, Figs. 2, 5, and 6 – they have the same structure, therefore, they have the same gain).

Regarding claim 23, Joffe discloses a circuit comprising an output terminal for connection to a load (45); an amplifier arrangement (20) having an output terminal and inverting and non-inverting input terminals (21-22), the amplifier arrangement being arranged for deriving at the output terminal thereof an output voltage having a magnitude directly proportional to the difference in the voltages at the inverting and non-inverting output terminals; first and second voltage dividers (31/34; 32/35); a sensing resistor (33) connected between the circuit output terminal and the amplifier arrangement output terminal; a first feedback path (upper or lower path) connected between the output terminal of the amplifier arrangement and one of the input terminals of the amplifier arrangement; a second feedback path (lower or upper path) connected between the output terminal of the circuit and the other input terminal of the amplifier

arrangement; the first feedback circuit being included in a first resistive voltage divider (31/34 or 32/35) connected between the circuit input terminal and the output terminal of the amplifier arrangement; the second feedback circuit being included in a second resistive voltage divider (32/35 or 31/34) connected between a further terminal and the circuit output terminal; the first voltage divider having a first tap (21 or 22) connected to drive the first input terminal of the amplifier arrangement; the second voltage divider having a second tap (22 or 21) connected to drive the second input terminal of the amplifier arrangement; the voltage dividers having voltage division factors and the sensing resistor having a value for causing the current flowing through the circuit output terminal into the load to be directly proportional to the difference in the voltages at the circuit input terminal and the further terminal; the laser diode (45) having first and second electrodes respectively connected to be responsive to the voltage of a non-grounded terminal of a DC voltage source and the circuit output terminal, the DC voltage source polarity and the laser diode polarity being such that DC current is adapted to flow between the DC voltage source ungrounded terminal and the circuit output terminal via the laser diode (see and compare the inventive Fig. 4 and the prior art figures, Figs. 2, 5, and 6 – they have the same structure).

Regarding claim 24, Joffe discloses the further terminal (the left side of the resister 31) is connected to ground and the circuit input terminal is connected to a voltage source.

Regarding claim 25, Joffe discloses the further (the left side of the resister 31) and input terminals are respectively connected to first and second voltage sources (240 of Fig. 7).

Regarding claim 26, Joffe discloses the amplifier arrangement of claim 23 is arranged so the gain factor polarity between inverting and non-inverting input terminals and the output terminals of the amplifier arrangement causes the output current of the amplifier arrangement to be directly proportional to and have the same polarity as (V.sub.A-V.sub.B), where V.sub.A and V.sub.B are respectively the voltages at the non-inverting and inverting input terminals (see and compare the inventive Fig. 4 and the prior art figures, Figs. 2, 5, and 6 – they have the same structure, therefore, they have the same gain).

Regarding claim 27, Joffe discloses a circuit comprising an output terminal (43) for connection to a load (45); an amplifier arrangement (20) having an output terminal and inverting and non-inverting input terminals (21-22), the amplifier arrangement being arranged for deriving at the output terminal thereof an output voltage having a magnitude directly proportional to the difference in the voltages at the inverting and non-inverting output terminals; first and second voltage dividers; a sensing resistor (33) connected between the circuit output terminal and the amplifier arrangement output terminal; a first feedback path (upper or lower path) connected between the output terminal of the amplifier arrangement and one of the input terminals of the amplifier arrangement; a second feedback path (lower or upper path) connected between the output terminal of the circuit and the other input terminal of the amplifier arrangement;

the first feedback circuit being included in a first resistive voltage divider (31/34 or 32/35) connected between the circuit input terminal and the output terminal of the amplifier arrangement; the second feedback circuit being included in a second resistive voltage divider (32/35 or 31/34) connected between a further terminal and the circuit output terminal; the first voltage divider having a first tap connected to drive the first input terminal of the amplifier arrangement; the second voltage divider having a second tap connected to drive the second input terminal of the amplifier arrangement; the voltage dividers having voltage division factors and the sensing resistor having a value for causing the current flowing through the circuit output terminal into the load to be directly proportional to the difference in the voltages at the circuit input terminal and the further terminal; the resistance (R.sub.1) of the first voltage divider between the output and first input terminal of the amplifier arrangement being of the same order of magnitude as the resistance of the second voltage divider between the circuit output terminal and the second terminal of the amplifier arrangement, the resistance (R.sub.2) of the first voltage divider between the first input terminal of the amplifier arrangement and the circuit input terminal being of the same order of magnitude as the resistance between the second input terminal of the amplifier arrangement (column 3, line 42; column 4, lines 61-65; and Fig. 2).

Regarding claim 28, Joffe discloses the R.sub.1 is much greater than the resistance of the sensing resistor (column 3, line 42).

Regarding claim 28, Joffe discloses the further terminal (the left side of the resister 31) is connected to ground and the circuit input terminal is connected to a voltage source (40).

Regarding claim 30, Joffe discloses the further terminal (the left side of the resister 31) and the input terminal are respectively connected to the first and second voltage sources having values that are not zero (240).

Regarding claim 31, Joffe discloses the amplifier arrangement is arranged so the gain factor polarity between inverting and non-inverting input terminals and the output terminals of the amplifier arrangement causes the output current of the amplifier arrangement to be directly proportional to and have the same polarity as (V.sub.A-V.sub.B), where V.sub.A and V.sub.B are respectively the voltages at the non-inverting and inverting input terminals (see and compare the inventive Fig. 4 and the prior art figures, Figs. 2, 5, and 6 – they have the same structure, therefore, they have the same gain).

Regarding claim 32, Joffe discloses the load (45) includes a laser diode having first and second electrodes respectively connected to be responsive to the voltage of a non-grounded terminal of a DC voltage source and the circuit output terminal, the DC voltage source polarity and the laser diode polarity being such that DC current is adapted to flow between the DC voltage source ungrounded terminal and the circuit output terminal via the laser diode.

Regarding claim 33, Joffe discloses the amplifier arrangement is arranged so the gain factor polarity between inverting and non-inverting input terminals and the output

terminals of the amplifier arrangement causes the output current of the amplifier arrangement to be directly proportional to and have the same polarity as (V.sub.A-V.sub.B), where V.sub.A and V.sub.B are respectively the voltages at the non-inverting and inverting input terminals (see and compare the inventive Fig. 4 and the prior art figures, Figs. 2, 5, and 6 – they have the same structure, therefore, they have the same gain).

Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclose (see the cited references on the USPTO-892 Form attached).

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN
June 7, 2005

PEGUY JEANPIERRE
PRIMARY EXAMINER